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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,711	07/28/2003	Irfan Rahim	009818-0076-999	6759
48591	7590	09/30/2005	EXAMINER	
MORGAN, LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE WASHINGTON, DC 20004			CHAN, EMILY Y	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/628,711

Applicant(s)

RAHIM ET AL.

Examiner

Emily Y. Chan

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 15 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 15-17 and 20-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-17 and 20-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 15-17 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al US Patent No. 6,683,767 in view of Koshikawa et al US Patent No. 5,319,302.

With respect to claims 15 and 22, Ito et al ('767) disclose a voltage regulator for providing an operating voltage to an integrated circuit (see Figs 1 and 27-28) as claimed, comprising:

a voltage down-converter (150-157) arranged to convert a chip-external supply voltage ( $V_{ext}$ ) to a converted voltage ( $V_{int}$ ) based on a signal indicative of a desired value of the converted voltage and output the converted voltage as the operating voltage; and

an adjustable signal generator (60, 100) for adjustably generating the signal indicative of the desired value of the converted voltage (see Col. 3, lines 23-28).

Ito et al ('767) do not disclose a detector for measuring at least one electrical or operational parameter of the integrated circuit and an evaluator to determine the desired value of the operating voltage based on the parameter(s) measured by the detector.

Koshikawa et al ('302) disclose a single semiconductor chip (10) comprising an internal voltage regulator unit (12) for semiconductor integrated circuit device as claimed and exclusively teach that internal voltage regulator unit (12) comprises a detector and evaluator to determine the desired value of the operating voltage based on the parameter(s) measured by the detector (see Figs 5 and 6, Col. 9, lines 8-46 and Abstract, last three lines " thereby allowing the internal power source to adjust the internal power voltage level to an arbitrary point").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate Koshikawa et al ('302)'s detector and evaluator into Ito et al ('767) 's voltage regulator for the expected benefit of providing the voltage regulating unit which improves stability of an internal power voltage level regardless of an external power voltage level as disclosed by Koshikawa et al ('302) (see Col. 7, lines 36-40).

With respect to claims 16 and 23, Ito et al ('767) disclose the voltage regulator (150-157) is an on-chip voltage regulator.

With respect to claims 17 and 24, Ito et al ('767) disclose that their adjustable signal generator (60, 100) is implemented in a programmable logic device (see Figs. 29-30).

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With respect to claim 20, Koshikawa et al ('302)'s evaluator is implemented in a programmable logic device (see Figs. 5 and 6).

With respect to claim 21, Ito et al ('767) 's reference circuit structures are circuit structure of the integrated circuit (See Col. 2, lines 25-27, "third area for laying first internal circuit which operate based on the internal power voltage").

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bryson US Patent No. 5,864,225 discloses a dual adjustable voltage regulator comprising means for automatically detecting and generating power supply voltage level as required by the system (see Abstract).

Wong US Patent No. 6,541,948 discloses a voltage regulator formed on an integrated circuit.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 15 and 22 have been considered but are moot in view of the new ground(s) of rejection.

### ***Response to Amendment***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Conclusion**


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

9-28-05

  
VINH NGUYEN  
PRIMARY EXAMINER  
A-U-2829  
09/29/05